PATENT ABSTRACTS OF JAPAN

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(51)Int.Cl. **H02M 1/08**

(21)Application number : **02-295512**

(22)Date of filing : **02.11.1990**

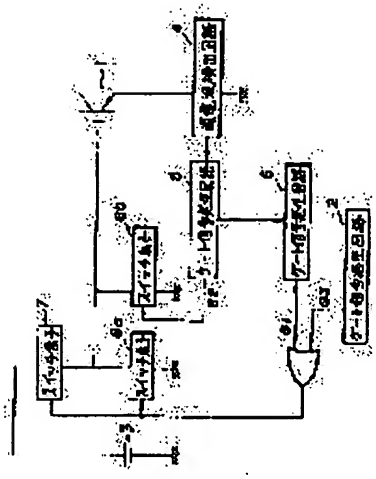
(71)Applicant : **HITACHI LTD**

(72)Inventor : **SAKURAI NAOKI**
MORI MUTSUHIRO
MIYAZAKI HIDEKI

(54) IGBT DRIVING CIRCUIT

(57)Abstract:

PURPOSE: To obtain a highly reliable IGBT driving circuit which can be integrated easily on a circuit board and causes no erroneous operation due to noise by sequentially lowering the gate voltage to zero when an overcurrent endures for longer than a predetermined interval.



CONSTITUTION: If an overcurrent detecting circuit 4 detects an overcurrent when an IGBT1 is turned ON, a detection signal is delivered to a gate signal generating circuit 5. When the overcurrent detecting circuit 4 delivers signals for longer than a predetermined time, the circuit 5 turns a switch element 8b ON based on a gate signal G2. Consequently, the IGBT1 has a gate voltage determined by a voltage bearing ratio which is determined by the ON resistance ratio between switch elements 7 and 8b. The gate signal generating circuit 5 also delivers a signal to a gate signal generating circuit 6. The circuit 6 holds the signal delivered from the circuit 5 for a predetermined interval and subsequently delivers a gate signal G1 for turning the elements 7 and 8b, respectively, OFF and ON thus bringing the gate signal to be applied on the IGBT1 to zero.

LEGAL STATUS

[Date of request for examination]

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[Date of final disposal for application]

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[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

PATENT FAMILY SEARCH FOR JP 04-172962

Subaccount 13361-049JP1

SOURCES:

Selected file: PLUSPAT
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Comprehensive Worldwide Patents database
Individual records for each Country or Patent Office
Coverage: 75 patenting authorities; start dates vary from 1800 forward
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Now available: Citations / Search Reports for German (DE) documents
Last update of file: 2006/02/22 (YYYY/MM/DD) 2006-07/UP (last update)

Selected file: WPAT
Derwent World Patents Index, (c) Thomson Scientific
UP (basic), UE(equiv), UA (poly), UB (chem) : updates through 2006-12
Manual Code Revision 2006 - final lists available on Thomson Scientific
Website. Revised codes will be implemented in the first update of 2006.
Please review lists to update manual codes in SDIs and stored searches.
Last database update : 2006/02/18 (YYYY/MM/DD)

Selected file: INPD
INPADOC International Patent Documentation Center
Source: European Patent Office - EPIDOS
Individual publication stage records for each Patenting Authority
Coverage: 75 patent offices ; start dates vary from 1968 forward
Current through weekly update 2006-07/up ; last update 2006/02/17
IPC Classes: for searching prior to 2006, use the qualifier: /IC
For searching IPC v8 (pd>=2006), use the qualifiers: /ICAA /ICCA

Selected file: USPAT
US Patents Full Text of United States Patent and Trademark Office
Coverage : 1971 to present (2006-08/UP)
Last database update : 2006/02/21 (YYYY/MM/DD)
For complete file information : see INFO USPAT
NEW 09/09/03 Kind Code for US Design patents from D to S1

Selected file: USAPPS
US Patent Applications full-text from USPTO (c) Questel.Orbit
Coverage: from beginning of Pre-Grant publication in March 2001
Reloaded: FactSheet on web. Pricing, see: INFO USAPPS
Last database update: 2006/02/23 (YYYY/MM/DD) 2006-08/UP

Selected file: IFIPAT
IFIPAT Claims/US Patents (c) IFI /CLAIMS(R) Patent Services
Thru PGP pd=2006-02-16 (2006-07/uap); Grant PD=2006-02-21 (2006-08/up)
Std Biblio thru PGP PD=2001-11(2002-11/uam);Grant PD=2005-06(2006-02/UM)
Chem Indxg thru PGP PD=2004-06(2006-02/uab);Grant PD=2005-10(2006-02/UB)
Reloaded 01/15/04 with Updated US Classes, & Business Terms(/BT)
From 06/04 forward questionable source data received from USPTO shows
PCT filing date, not date of national stage as app date for US patents
that entered via PCT route. IFI is investigating.

EPO REGISTER

PATOLIS-e

PATENT FAMILY

#	Patent No.	Kind	Date	Applic.No.	Date
1)	EP-483744	A2	19920506	1991EP-0118397	19911029
	EP-483744	A3	19930317		
2)	JP04172962	A	19920619	1990JP-0295512	19901102
	JP2892815	B2	19990517		
3)	JP04190676	A	19920709	1990JP-0316754	19901121
	JP2696270	B2	19980114		

Priority :
1990JP-0295512 19901102
1990JP-0316754 19901121

SEARCH RESULTS:

1 / 3 PLUSPAT - ©QUESTEL-ORBIT - image

Patent Number :
EP0483744 A2 19920506 [EP-483744]
Publication Stage :
(A2) Pub. Of applic. Without search report
Title :
(A2) Current detection circuit of power semiconductor device and power converter using the circuit.
Other Title :
(A2) Stromdetektorschaltung für Leistungshalbleiteranordnung und die Schaltung benutzender Leistungswandler.
(A2) Circuit de détection de courant pour un dispositif semi-conducteur de puissance et convertisseur de puissance employant ce circuit.
Patent Assignee :
(A2) HITACHI LTD (JP)
Inventor(s) :
(A2) MIYAZAKI HIDEKI (JP); WATANABE KOUZOU (JP); ONDA KENICHI (JP); TANAKA TOMOYUKI (JP); SAKURAI NAOKI (JP); MORI MUTSUHIRO (JP)
Intl Patent Class :
(A2) G01R-019/165 H02H-003/087 H02M-007/537 H03K-017/08
Patent Number 2 :
EP0483744 A3 19930317 [EP-483744]
Publication Stage 2 :
(A3) Publi. Of search report
Title 2 :
(A3) CURRENT DETECTION CIRCUIT OF POWER SEMICONDUCTOR DEVICE AND POWER CONVERTER USING THE CIRCUIT
Intl Patent Class 2 :
(A3) H02M-007/537
Language :
ENGLISH (ENG)
Application Nbr :
EP91118397 19911029 [1991EP-0118397]
Priority Details :
JP29551290 19901102 [1990JP-0295512]
JP31675490 19901121 [1990JP-0316754]
EPO ECLA Class :
G01R-019/165H2B
G01R-019/165H5B
G01R-019/175
H02M-003/156B
H02M-007/5387C3
H03K-017/082B
H03K-017/082E
Designated States :
DE GB

Document Type :
Basic

1 / 1 LEGALI - ©EPO
Patent Number :
EP0483744 A2 19920506 [EP-483744]EP0483744 A3 19930317 [EP-483744]
Application Number :
EP91118397 19911029 [1991EP-0118397]
Action Taken :
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BENANNTE VERTRAGSSTAATEN
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REQUEST FOR EXAMINATION FILED
PRUEFUNGSANTRAG GESTELLT
EFFECTIVE DATE: 19911029

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19930428 EP/18W-A [-]
WITHDRAWN
ZURUECKGENOMMEN
WITHDRAWAL DATE: 19930215
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2003-22

2 / 3 PLUSPAT - ©QUESTEL-ORBIT - image
Patent Number :
JP4172962 A 19920619 [JP04172962]
Publication Stage :
(A) Doc. Laid open to publ. Inspec.
Title :
(A) IGBT DRIVING CIRCUIT
Patent Assignee :
(A) HITACHI LTD
Patent Assignee :
(A) HITACHI LTD
Inventor(s) :
(A) SAKURAI NAOKI; MORI MUTSUHIRO; MIYAZAKI HIDEKI
Intl Patent Class :
(A) H02M-001/00 H02M-001/08 H02M-001/08 H03K-017/04 H03K-017/56
Patent Number 2 :
JP2892815 B2 19990517 [JP2892815]
Publication Stage 2 :
(B2) Grant. Pat. With A from 2500000 on
Intl Patent Class 2 :
(B2) H02M-001/08
Application Nbr :
JP29551290 19901102 [1990JP-0295512]
Priority Details :
JP29551290 19901102 [1990JP-0295512]

3 / 3 PLUSPAT - ©QUESTEL-ORBIT - image

Patent Number :
JP4190676 A 19920709 [JP04190676]
Publication Stage :
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Title :
(A) CURRENT DETECTION CIRCUIT FOR POWER SEMICONDUCTOR ELEMENT AND POWER CONVERSION DEVICE USING SAME
Patent Assignee :
(A) HITACHI LTD
Patent Assignee :
(A) HITACHI LTD
Inventor(s) :
(A) MIYAZAKI HIDEKI; WATANABE KOZO; ONDA KENICHI; TANAKA TOMOYUKI
Intl Patent Class :
(A) H02M-001/08
Patent Number 2 :
JP2696270 B2 19980114 [JP2696270]
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(B2) Grant. Pat. With A from 2500000 on
Intl Patent Class 2 :
(B2) H02M-001/08 H02M-007/00
Application Nbr :
JP31675490 19901121 [1990JP-0316754]
Priority Details :
JP31675490 19901121 [1990JP-0316754]

EP/PCT LEGAL STATUS INFORMATION FROM THE EPO REGISTER

Online European Patent Register - Results

Status of the database as of 21-02-2006 (dd-mm-yyyy)

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Publication numbers, publication type and publication dates
EP0483744 A2 06-05-1992 [1992/19]
EP0483744 A3 17-03-1993 [1993/11]

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Date of publication of search report 17-03-1993 [1993/11]

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JP19900295512 02-11-1990;
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[
H02M7/537 [1992/19]
]

Designated states
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English title
Current detection circuit of power semiconductor device and power converter using the circuit [1992/19]

French title
Circuit de détection de courant pour un dispositif semi-conducteur de puissance et convertisseur de puissance employant ce circuit [1992/19]

German title
Stromdetektorschaltung für Leistungshalbleiteranordnung und die Schaltung benutzender Leistungswandler [1992/19]

Designated states, applicant name, address
FOR ALL DESIGNATED STATES
Hitachi, Ltd.
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Chiyoda-ku, Tokyo/JP [N /P]
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FOR ALL DESIGNATED STATES
HITACHI, LTD.
6, Kanda Surugadai 4-chome
Chiyoda-ku, Tokyo 100/JP [1992/19]
]

Inventor name, address
01 / Miyazaki, Hideki / 1-19-4-403, Ishinazaka-cho / Hitachi-shi,

Ibaraki-ken / JP
02 / Watanabe, Kouzou / 1-12-44, Minamikouya-cho / Hitachi-shi, Ibaraki-ken / JP
03 / Onda, Kenichi / 2-18-3, Daihara-cho / Hitachi-shi, Ibaraki-ken / JP
04 / Tanaka, Tomoyuki / 6-5-5, Omika-cho / Hitachi-shi, Ibaraki-ken / JP
05 / Sakurai, Naoki / 6-20-3, Ayukawa-cho / Hitachi-shi, Ibaraki-ken / JP
06 / Mori, Mutsuhiro / 1-19-4-203, Ishinazaka-cho / Hitachi-shi, Ibaraki-ken / JP [1992/19]

Representative name, address

Altenburg, Udo, Dipl.-Phys., et al
Patent- und Rechtsanwälte Bardehle . Pagenberg . Dost . Altenburg .Geissler Galileiplatz 1
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Dossier destroyed 13-09-2003

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Application withdrawn or deemed to be withdrawn

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Documents cited in the European Search

EP0149749 A1 [ ];
EP0010980 A1 [ ];
JP23007828 A [ ]
[ ] RESEARCH DISCLOSURE, no. 309, January 1990, page 80, New
York US; "Active 10 AMP current limit circuit for smartpower applications"
[ ] PATENT ABSTRACTS OF JAPAN vol. 14, no. 190 (E-918)(4133) 18
April 1990 & JP-A-23 7 828 (FUJI) 7 February 1990

[End of Data]

Return to Search Screen

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JAPANESE LEGAL STATUS INFORMATION FROM PATOLIS-e

** Result [P] ** Format(P803) 2006.02.24 1/ 1

Application No./Date: 1990-295512[1990/11/ 2]
Public Disclosure No./Date: 1992-172962 [1992/ 6/19]
Registration No./Date: 2892815 [1999/ 2/26]
Examined Publication Date (present law): [1999/ 5/17]
Examined Publication No./Date (old law): [ ]
PCT Application No.:
PCT Publication No./Date: [ ]
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Domestic Priority: [ ] ( )
Date of Request for Examination: [1997/10/ 1]
Accelerated Examination: ( )
Kind of Application: (0000)
Critical Date of Publication: [1990/11/ 2]( )
No. of Claims: (5)
Applicant: HITACHI LTD
Inventor: SAKURAI NAOKI,MORI MUTSUHIRO,MIYAZAKI HIDEKI
IPC: H02M 1/08 H02M 1/00 H02M 1/08 ,311
H03K 17/04 H03K 17/56
FI: H02M 1/08 A H02M 1/00 H H02M 1/08 ,311E
H03K 17/04 F H03K 17/56
F-Term: 5H740AA04,AA10,BA12,BB05,BB06,BB07,BB08,BC01,BC02,HH05,JA01,MM11,5J055 AX10,AX23,AX34,AX35,AX37,AX47,AX56,AX61,AX64,AX66,BX16,CX19,CX20,DX09,DX10,D X52,DX55,DX60,DX84,EX01,EX03,EX07,EX10,EX11,EX14,EX21,EY01,EY10,EY12,EY21,EY 29,EZ01,EZ07,EZ25,EZ32,EZ50,FX04,FX13,FX19,FX20,FX31,FX32,GX00,GX01,GX02,GX0 4,GX05
Expanded Classicication: 432
Fixed Keyword: R097
Citation: [, . . ,] (, ,)
Title of Invention: IGBT DRIVING CIRCUIT

Abstract: PURPOSE: To obtain a highly reliable IGBT driving circuit which can be integrated easily on a circuit board and causes no erroneous operatio n due to noise by sequentially lowering the gate voltage to zero when an ove rcurrent endures for longer than a predetermined interval. CONSTITUTION: If an overcurrent detecting circuit 4 detects an overcurrent when an IGBT1 is t urned ON, a detection signal is delivered to a gate signal generating circui t 5. When the overcurrent detecting circuit 4 delivers signals for longer th an a predetermined time, the circuit 5 turns a switch element 8b ON based on a gate signal G2. Consequently, the IGBT1 has a gate voltage determined by a voltage bearing ratio which is determined by the ON resistance ratio betwe en switch elements 7 and 8b. The gate signal generating circuit 5 also deliv ers a signal to a gate signal generating circuit 6. The circuit 6 holds the signal delivered from the circuit 5 for a predetermined interval and subsequ ently delivers a gate signal G1 for turning the elements 7 and 8b, respectiv ely, OFF and ON thus bringing the gate signal to be applied on the IGBT1 to zero.COPYRIGHT: (C)1992,JPO&Japio

Relation to Original Application: ( )
Original Application No.: (
)
Original Registration No.: ( )
Retroactive Date: [
]
Assignment/License: (0)
Classification of Examiners Decision/Date:
(decision of registration(allowance)) [1999/ 2/ 9]
Final Examinational Transaction/Date:
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Kind of Examination: (01)
Examination Intermediate Record:
(A63 1990/11/ 2,PATENT APPLICATIONUTILITY MODEL REGISTRATION APPLICATION, 1 4000:)(A23 1990/11/27,NOTICE OF APPLICATION NUMBER, :)
(A621 1997/10/ 1,WRITTEN REQUEST FOR EXAMINATION, 97800:)

(A752 1997/10/ 1,NOTIFICATION OF CHANGE IN SEAL (REPRESENTATIVE), :)
(A523 1997/10/ 1,WRITTEN AMENDMENT, :)
(A01 1999/ 2/ 9,DECISION TO GRANT A PATENTDECISION OF REGISTRATION, :
)(A61 1999/ 2/22,PAYMENT OF ANNUAL FEE, :)

*** Trial No./Date: [ ]
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Defendand: -
Opponent: -
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No. of Opposition Claims: ( )( )
Classification of Trial Decision of Opposition/Date:
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Final Disposition of Trial or Appeal/Date:
( ) [ ]
Trial and Opposition Intermediate Record:

Registration Intermediate Record:
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(R100 1999/ 2/22,A WRITTEN PAYMENT FOR ESTABLISHMENT, :01)
(R150 1999/ 3/ 5,A REGISTRATION CERTIFICATE, :01)
(R20 2002/ 1/29,A WRITTEN ANNUITY PAYMENT, :02)
(R2501 2002/ 6/25,A RECEIPT OF ANNUITY PAYMENT (LUMP SUM PAYMENT), :02)
(R20 2003/ 1/28,A WRITTEN ANNUITY PAYMENT, :03)
(R2501 2003/ 2/18,A RECEIPT OF ANNUITY PAYMENT (LUMP SUM PAYMENT), :03)
(R20 2004/ 1/27,A WRITTEN ANNUITY PAYMENT, :04)
(R2501 2004/ 2/10,A RECEIPT OF ANNUITY PAYMENT (LUMP SUM PAYMENT), :04)
(R20 2005/ 1/27,A WRITTEN ANNUITY PAYMENT, :05)
(R2501 2005/ 2/15,A RECEIPT OF ANNUITY PAYMENT (LUMP SUM PAYMENT), :05)
Amount of Annuity Payment: (7Years)
Extinction of Right/Lapse Date of Right:
()[ ]
Closed Register Filing Date: [ ]
Proprietor: 13-HITACHI LTD
Status of Register: ( )

** Result [P] ** Format(P803) 2006.02.24 1/ 1

Application No./Date: 1990-316754[1990/11/21]
Public Disclosure No./Date: 1992-190676 [1992/ 7/ 9]
Registration No./Date: 2696270 [1997/ 9/19]
Examined Publication Date (present law): [1998/ 1/14]
Examined Publication No./Date (old law): [ ]
PCT Application No.:
PCT Publication No./Date: [ ]
Preliminary Examination: ()
Priority Country/Date/No.: ( ) [ ] ( )
Domestic Priority: [ ] ( )
Date of Request for Examination: [1994/ 8/23]
Accelerated Examination: ( )
Kind of Application: (0000)
Critical Date of Publication: [1990/11/21]( )
No. of Claims: (11)
Applicant: HITACHI LTD
Inventor: MIYAZAKI HIDEKI,WATANABE KOZO,ONDA KENICHI,TANAKA TOMOYUKI
IPC: H02M 1/08
FI: H02M 7/00 H02M 1/08 A H02M 7/12 G
H02M 7/12 H
F-Term: 5H740AA10,BA11,BA12,BB05,BB06,BB07,BB09,BB10,BC01,BC02,HH05,JA01,JA09,MM01,MM11,MM14,MM08,5H006AA03,AA05,AA06,BB00,CA01,CB01,CB03,CC02,CC08,DC02,DC08,FA02,FA03,GA04
Expanded Classicication: 432,422
Fixed Keyword: R097
Citation: [, . . ,] (, ,)
Title of Invention: CURRENT DETECTION CIRCUIT FOR POWER SEMICONDUCTOR ELEMENT AND POWER CONVERSION DEVICE USING SAME

Abstract: PURPOSE: To make electric currents detectable at a plurality of detecting levels so as to reduce the occurrence of losses by making a reference current corresponding to one of the detecting levels to flow to the main circuit of each transistor of a comparator circuit and a control current of a level correlative to a load current to flow to a control circuit. CONSTITUTION: A reference current of a value corresponding to one of detecting levels is made to flow to the main circuit of each transistor of a comparator circuit and a control current Ir of a level correlative to a load current IL is made to flow to a control circuit 6. When the control current Ir becomes larger than the reference current, the potential VS_1 and VS_2 at connecting points between the transistors and a current source drop to nearly zero and the load current IL detects that a prescribed detecting level is exceeded. In addition, the load current is detected at a plurality of detecting levels by making the level of the reference current made to flow to each transistor to correspond to the detecting levels.COPYRIGHT: (C)1992,JPO&Japio

Relation to Original Application: ( )
Original Application No.: ( ).
Original Registration No.: ( )
Retroactive Date: [ ]
Assignment/License: (0)
Classification of Examiners Decision/Date:
(decision of registration(allowance)) [1997/ 7/29]
Final Examinational Transaction/Date:
(registration) [1997/ 9/19]
Kind of Examination: (01)
Examination Intermediate Record:
(A63 1990/11/22,PATENT APPLICATIONUTILITY MODEL REGISTRATION APPLICATION, 14000:)(A23 1990/12/14,NOTICE OF APPLICATION NUMBER, :)
(A7D2 1991/ 1/10,NOTIFICATION OF LUMP CHANGE IN DOMICILE (REPRESENTATIVE), :)
(A7D2 1991/10/11,NOTIFICATION OF LUMP CHANGE IN DOMICILE (REPRESENTATIVE), :)(A621 1994/ 8/24,WRITTEN REQUEST FOR EXAMINATION, 114000:)
(A523 1994/ 8/24,WRITTEN AMENDMENT, :)
(A7D2 1994/10/ 5,NOTIFICATION OF LUMP CHANGE IN DOMICILE (REPRESENTATIVE), :)
(A7D2 1995/ 5/ 1,NOTIFICATION OF LUMP CHANGE IN DOMICILE (REPRESENTATIVE), :)
(A7D2 1995/ 5/ 1,NOTIFICATION OF LUMP CHANGE IN DOMICILE (REPRESENTATIVE),

:)
(A7D2 1995/ 5/ 1,NOTIFICATION OF LUMP CHANGE IN DOMICILE (REPRESENTATIVE),
:)
(A01 1997/ 7/29,DECISION TO GRANT A PATENTDECISION OF REGISTRATION, :
)(A61 1997/ 8/21,PAYMENT OF ANNUAL FEE, :)

*** Trial No./Date: [ ]
Kind of Trial: [ ] ***
Demandant: -
Defendand: -
Opponent: -
No. of Opposition in Effect: ( )
No. of Opposition Claims: ( )( )
Classification of Trial Decision of Opposition/Date:
( ) [ ]
Final Disposition of Trial or Appeal/Date:
( ) [ ]
Trial and Opposition Intermediate Record:

Registration Intermediate Record:
(R01 1997/ 7/29,A NOTICE OF DECISION OF REGISTRATION, :01)
(R100 1997/ 8/20,A WRITTEN PAYMENT FOR ESTABLISHMENT, :01)
(R150 1997/ 9/29,A REGISTRATION CERTIFICATE, :01)
(R20 2000/ 8/30,A WRITTEN ANNUITY PAYMENT, :02)
(R2501 2000/10/17,A RECEIPT OF ANNUITY PAYMENT (LUMP SUM PAYMENT), :02)
Amount of Annuity Payment: (4Years)
Extinction of Right/Lapse Date of Right:
(non-payment of annual fee) [2001/ 9/19]
Closed Register Filing Date: [2002/ 5/29]
Proprietor: 13-HITACHI LTD
Status of Register: (removed to closed register)